UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/585,643	07/07/2006	**Takanori Okada**	056937-0295	5463

53080 7590 11/09/2009

MCDERMOTT WILL & EMERY LLP
600 13TH STREET, NW
WASHINGTON, DC 20005-3096

EXAMINER	
GIARDINO JR, MARK A	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
11/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/585,643	OKADA ET AL.	
	Examiner	Art Unit	
	MARK A. GIARDINO JR	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2,4,8,10,14 and 16* is/are allowed.

6)☒ Claim(s) *1, 3, 5-7, 9, 11-13, and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/12/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The Examiner acknowledges the applicant's submission of the amendment dated 6/26/2009. At this point claims 5, 11, and 17 have been amended. Thus, claims 1-18 are pending in the instant application.

The instant application having Application No. 10/585,643 has a total of 18 independent claims pending in the application.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

The information disclosure statement filed 5/12/2009 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each reference listed that is not in the English language. It has been placed in the application file, but the Japanese Office Action therein has not been considered.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. ' 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 6, 12, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Chiba (US 6,401,166).

Regarding Claim 6, Chiba teaches a non-volatile semiconductor recording medium **(memory card 40 of Figure 3)** in which information is recorded according to a recording format of FAT file system **(Chiba uses the FAT file system, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

wherein a user data region comprising a plurality of clusters **(data regions of Figure 4, which also shows a plurality of clusters among the data regions)** and a file allocation table region **(FAT region of Figure 4)** are included in the FAT file system;

an information on a state of each cluster in the user data region is recorded in the file allocation table region **(since the CPU can tell if a cluster is empty by analyzing the content of the FAT, the FAT inherently records information on the state of the clusters, Column 14 Lines 3-4)**;

the file allocation table region indicates that a continuous series of at least three clusters each has a state value indicating a cluster is not to be written to because it is a defective cluster, a reserved cluster or an already-used cluster **(the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-4, also see step S504 of Figure 11, and if three continuous clusters are used, the file allocation table region indicates that a continuous series of at least three clusters are used)**,

and a region of the user data region corresponding to the continuous series of at

least three clusters is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25)**.

Regarding Claim 12, Chiba teaches a method of recording information in a non-volatile semiconductor recording medium **(memory card 40 of Figure 3)** in which information is recorded according to a recording format of FAT file system **(Chiba uses the FAT file system, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

wherein a user data region comprising a plurality of clusters **(data regions of Figure 4, which also shows a plurality of clusters among the data regions)** and a file allocation table region **(FAT region of Figure 4)** are included in the FAT file system;

an information on a state of each cluster in the user data region is recorded in the file allocation table region **(since the CPU can tell if a cluster is empty by analyzing the content of the FAT, the FAT inherently records information on the state of the clusters, Column 14 Lines 3-4)**;

the file allocation table region indicates that a continuous series of at least three clusters each has a state value indicating a cluster is not to be written to because it is a defective cluster, a reserved cluster or an already-used cluster **(the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is**

empty, Column 14 Lines 3-4, also see step S504 of Figure 11, and if three continuous clusters are used, the file allocation table region indicates that a continuous series of at least three clusters are used),

and a region of the user data region corresponding to the continuous series of at least three clusters is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25)**.

Regarding Claim 18, Chiba teaches an information recording format for a non-volatile semiconductor recording medium **(memory card 40 of Figure 3)** in which information is recorded according to a recording format of FAT file system **(Chiba uses the FAT file system, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

wherein a user data region comprising a plurality of clusters **(data regions of Figure 4, which also shows a plurality of clusters among the data regions)** and a file allocation table region **(FAT region of Figure 4)** are included in the FAT file system;

an information on a state of each cluster in the user data region is recorded in the file allocation table region **(since the CPU can tell if a cluster is empty by analyzing the content of the FAT, the FAT inherently records information on the state of the clusters, Column 14 Lines 3-4)**;

the file allocation table region indicates that a continuous series of at least three clusters each has a state value indicating a cluster is not to be written to because it is a defective cluster, a reserved cluster or an already-used cluster **(the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-4, also see step S504 of Figure 11, and if three continuous clusters are used, the file allocation table region indicates that a continuous series of at least three clusters are used)**,

and a region of the user data region corresponding to the continuous series of at least three clusters is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and at the end of the process of Figure 10 the master boot region is created while the other regions remain in a state where data is physically erased, see Format processing information on Column 12 Line 52 to Column 13 Line 25)**.

Claim Rejections - 35 USC ' 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 7, 9, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Chiba (US 6,401,166) in view of Briner et al (US 6,591,327).**

Regarding Claim 1, Chiba teaches a recording medium of non-volatile semiconductor **(memory card 40 of Figure 3)** comprising:

a plurality of blocks, each block being a first size **(the blocks corresponding to the pages shown on Figure 4 of Chiba)**;

a partition management information region **(master boot memory region of Figure 4 in Chiba)** and

a partition region **(starting with partition boot memory region of Figure 4)**, wherein

an information on a start position of the partition region is recorded in the partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**,

the start position information includes a value at which a predetermined region **(the predetermined region being the "empty region" of Figure 4)** is secured between a terminal end of the partition management information region and a starting end of the partition region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition [including the empty region] begins and ends, Column 8 Lines 27-32)**, and

the region secured between the terminal end of the partition management information region is larger than the first size **(Figure 4 clearly shows the empty region as 14 pages long, which is thus larger than the first size)** and the starting end of the partition region is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to units within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 3, Chiba teaches a non-volatile semiconductor recording medium **(flash memory 1 of Figure 1)** comprising:

a plurality of erasing blocks, each erasing block being of a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**; wherein

information is recorded according to a recording format of a predetermined file

system **(FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

a region which is not used for the recording is larger than the first size included in the recording format of the file system **("empty region" of Figure 4, which is used "for coinciding a head and end of the block...with those of a cluster", and is thus not used for the recording, Column 8 Lines 34-38, also Figure 4 clearly shows the empty region as 14 pages long, which is thus larger than the first size)**, and the region which is not used for the recording is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to sectors within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 7, Chiba teaches a method of recording information in a non-

volatile semiconductor **(memory card 40 of Figure 3)** comprising:

a plurality of blocks, each block being a first size **(the blocks corresponding to the pages shown on Figure 4 of Chiba)**;

a partition management information region **(master boot memory region of Figure 4 in Chiba)** and

a partition region **(starting with partition boot memory region of Figure 4)**, wherein

an information on a start position of the partition region is recorded in the partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**,

the start position information includes a value at which a predetermined region **(the predetermined region being the "empty region" of Figure 4)** is secured between a terminal end of the partition management information region and a starting end of the partition region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition [including the empty region] begins and ends, Column 8 Lines 27-32)**, and

the region secured between the terminal end of the partition management information region is larger than the first size **(Figure 4 clearly shows the empty region as 14 pages long, which is thus larger than the first size)** and the starting

end of the partition region is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to units within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 9, Chiba teaches a method of recording information in a non-volatile semiconductor recording medium **(flash memory 1 of Figure 1)** comprising:

a plurality of erasing blocks, each erasing block being of a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**; wherein

information is recorded according to a recording format of a predetermined file system **(FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

a region which is not used for the recording is larger than the first size included in

the recording format of the file system **("empty region" of Figure 4, which is used "for coinciding a head and end of the block...with those of a cluster", and is thus not used for the recording, Column 8 Lines 34-38, also Figure 4 clearly shows the empty region as 14 pages long, which is thus larger than the first size)**, and the region which is not used for the recording is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to sectors within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 13, Chiba teaches an information recording format for a non-volatile semiconductor recording medium **(memory card 40 of gure 3)** comprising:

a plurality of blocks, each block being a first size **(the blocks corresponding to the pages shown on Figure 4 of Chiba)**;

a partition management information region **(master boot memory region of Figure 4 in Chiba)** and

a partition region **(starting with partition boot memory region of Figure 4)**, wherein

an information on a start position of the partition region is recorded in the partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**,

the start position information includes a value at which a predetermined region **(the predetermined region being the "empty region" of Figure 4)** is secured between a terminal end of the partition management information region and a starting end of the partition region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition" and the "position of an end page of each partition" and thus contains a value indicating where each partition [including the empty region] begins and ends, Column 8 Lines 27-32)**, and

the region secured between the terminal end of the partition management information region is larger than the first size **(Figure 4 clearly shows the empty region as 14 pages long, which is thus larger than the first size)** and the starting end of the partition region is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where**

data is physically erased).

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to units within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 15, Chiba teaches an information recording format for non-volatile semiconductor recording medium **(flash memory 1 of Figure 1)** comprising:

a plurality of erasing blocks, each erasing block being of a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**; wherein

information is recorded according to a recording format of a predetermined file system **(FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

a region which is not used for the recording is larger than the first size included in the recording format of the file system **("empty region" of Figure 4, which is used "for coinciding a head and end of the block...with those of a cluster", and is thus not used for the recording, Column 8 Lines 34-38, also Figure 4 clearly shows the**

empty region as 14 pages long, which is thus larger than the first size), and the region which is not used for the recording is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to sectors within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Claims 5, 11, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiba and Briner in view of Nakamura et al (US 6,873,789).

Regarding Claim 5, Chiba teaches a non-volatile semiconductor recording medium of non-volatile semiconductor **(flash memory 1 of Figure 1)** comprising:

a plurality of blocks, each block being a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**;

A partition management information region **(master boot memory region of**

Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26);

and a partition containing a file system specific region **(Chriba uses the FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition", Column 8 Lines 30-32)**,

the partition comprises a partition descriptor information region **(partition boot memory region of Figure 4)**;

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**;

the start position information includes a value at which a predetermined region of a plurality of memory blocks **("empty region" of Figure 4, composed of multiple pages [blocks] of memory as shown on Figure 4)** is secured prior to a starting end of the file system specific region region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**, and

the region secured prior to the starting end of the space bit map region **(the**

empty region is shown between the boot information region and file allocation table region in Figure 4) is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chriba does not teach using the UDF file system with a space bit map region. Nakamura teaches a UDF file system **(Column 6 Lines 22-25)** with a space bit map in memory **(Column 12 Lines 52-53)**. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used the space bit map for the file system specific region of Chriba and to use a UDF file system in place of the FAT file system, so that the memory device of Chriba can be compatible with operating systems that use the UDF file system.

Also, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to sectors within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 11, Chiba teaches a method of recording information in a non-volatile semiconductor recording medium of non-volatile semiconductor **(flash memory 1 of Figure 1)** comprising:

a plurality of blocks, each block being a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**;

A partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**;

and a partition containing a file system specific region **(Chriba uses the FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition", Column 8 Lines 30-32)**,

the partition comprises a partition descriptor information region **(partition boot memory region of Figure 4)**;

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**;

the start position information includes a value at which a predetermined region of a plurality of memory blocks **("empty region" of Figure 4, composed of multiple pages [blocks] of memory as shown on Figure 4)** is secured prior to a starting end of the file system specific region region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**, and

the region secured prior to the starting end of the space bit map region **(the empty region is shown between the boot information region and file allocation table region in Figure 4)** is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chriba does not teach using the UDF file system with a space bit map region. Nakamura teaches a UDF file system **(Column 6 Lines 22-25)** with a space bit map in memory **(Column 12 Lines 52-53)**. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have used the space bit map for the file system specific region of Chriba and to use a UDF file system in place of the FAT file system, so that the memory device of Chriba can be compatible with operating systems that use the UDF file system.

Also, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to sectors within a block

(Column 4 Lines 3-4 in Briner).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

Regarding Claim 17, Chiba teaches an information recording format for a non-volatile semiconductor recording medium **(flash memory 1 of Figure 1)** comprising:

a plurality of blocks, each block being a first size **(the blocks corresponding to pages of a fixed size, Column 5 Lines 49-51)**;

A partition management information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**;

and a partition containing a file system specific region **(Chriba uses the FAT file system format, which uses "a table indicating an allocation of the file", Column 8 Line 64)**,

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(the partition information in the master boot region contains information on the "position of a beginning page of each partition", Column 8 Lines 30-32)**,

the partition comprises a partition descriptor information region **(partition boot memory region of Figure 4)**;

an information on a start position of the space bit map region is recorded in the partition descriptor information region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**;

the start position information includes a value at which a predetermined region of a plurality of memory blocks **("empty region" of Figure 4, composed of multiple pages [blocks] of memory as shown on Figure 4)** is secured prior to a starting end of the file system specific region region **(master boot memory region of Figure 4, which contains "a region for recording information...of each partition provided on this memory", Column 8 Lines 21-26)**, and

the region secured prior to the starting end of the space bit map region **(the empty region is shown between the boot information region and file allocation table region in Figure 4)** is in a state where data is physically erased **(see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block", and the "empty region" remains in a state where data is physically erased)**.

However, Chriba does not teach using the UDF file system with a space bit map region. Nakamura teaches a UDF file system **(Column 6 Lines 22-25)** with a space bit map in memory **(Column 12 Lines 52-53)**. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject

matter pertains to have used the space bit map for the file system specific region of Chriba and to use a UDF file system in place of the FAT file system, so that the memory device of Chriba can be compatible with operating systems that use the UDF file system.

Also, Chiba does not teach the pages of Chiba as physically erasable as a single unit. Briner teaches the ability to adjust erasable sizes down to sectors within a block **(Column 4 Lines 3-4 in Briner)**.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to which the subject matter pertains to have implemented the adjustable erasable size (as in Briner) in the device of Chiba, thereby allowing units of data such as Chiba's page to be physically erased as a single unit, to facilitate erasing different types of data **(Column 1 Lines 32-36 in Briner)**. Thus, by combining the devices, additional benefits are obtained.

ARGUMENTS CONCERNING PRIOR ART REJECTIONS

Rejections - USC 102/103

Applicant's arguments regarding Claims 1, 7, and 13 on Page 15 of the submitted remarks that "the Office Action ignores that FIG. 4 shows a device in which the smallest erasable unit is a 16-page block, and that the size of the 14-page empty region is determined by the size of the erasable unit of the memory device" has been considered but is not persuasive. The language in the argument does not address the

limitations in the claimed invention nor the language of the Office Action, and is therefore moot.

Applicant's arguments regarding Claims 1, 7, and 13 that "if the Chiba device were modified as proposed by the Office Action, such that the smallest erasable unit was a page, no empty region would be required", as "the device would still obtain 'coinciding a head and end of the block which is a physical unit with those of a cluster which is a logical unit managed by the OS'" has been considered but is not persuasive. This argument does not address the motivation used in the Office Action, nor does it address the limitations in the claims and is therefore moot.

Applicant's argument regarding Claims 1, 7, and 13 on Pages 16-17 of the submitted remarks that "the modification of Chiba proposed by the Office Action does not succeed in demonstrating that...'the region...is larger than the first size" would have been obvious has been considered but is not persuasive. Claim 1 states that "each erasing block being a first size and physically erasable as a single unit", and the block corresponds to the sectors in the combined device, as they are physically erasable as a single unit, as shown on Column 4 Lines 3-4 in Briner. Some sections of the memory are erasable in sector units, and some sections are erasable in block units (the partitioning is changeable, Column 4 Lines 56-57 in Briner, and the memory is split into partitions as further described in Column 2 Lines 48-56 in Briner). Since the partition is changeable, all sectors are *physically* erasable as a single unit, and when the partition management information region recited in Claim 1 is allocated to the section erasable in 'blocks', the empty region is still required to align the start the FAT region, but the blocks

are still made up of sectors which are of a first size and physically erasable. Thus, the rejection has been maintained as the combination is obvious as recited in the rejection above.

Applicant's argument regarding Claims 6, 12, and 18 that "the FAT file system disclosed by Chiba does not satisfy both of the last paragraphs of claim 6" has been considered but is not persuasive. Chiba teaches erasing the user data region (see step s401 in Figure 10, where there is a command to "erase each block and then erase the storage content of each block") thus including a region of the user data region corresponding to the continuous series of at least three clusters. This satisfies the last paragraph.

During use, the clusters are used for file storage and the FAT can tell if a cluster is already used [or reserved] based on whether or not the cluster is empty, Column 14 Lines 3-4, also see step S504 of Figure 11, and if three continuous clusters are used, the file allocation table region would indicate that a continuous series of at least three clusters are used. This satisfies the second-to-last paragraph. The reference teaches the limitations of Claims 6, 12, and 18 to the extent that they are claimed.

CLOSING COMMENTS

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. ' 707.07(i)**:

SUBJECT MATTER CONSIDERED ALLOWABLE

Claims 2, 8, 14, 4, 10, and 16 have been considered allowable subject matter.

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1, 3, 5, 6, 7, 9, 11, 12, 13, 15, 17, and 18 have received a second action on the merits and are subject of a second action final.

DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to M. Anthony Giardino whose telephone number is (571)

270-3565 and can normally be reached on Monday - Thursday 7:30am – 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

M.A. Giardino

/M.G./

Patent Examiner
Art Unit 2185

/Stephen Elmore/
Primary Examiner, Art Unit 2185